Amendments to the Claims

Claim 1 **(Canceled)**

Claim 2 **(Currently Amended)** [The digital PLL device of Claim 1] A clock generation apparatus comprising:

A/D conversion means for converting an input analog signal into a digital signal;

arithmetic means for generating a threshold used as a reference when binarizing the digital signal to generate a binary signal and a synchronous clock for sampling the binary signal, on the basis of the digital signal;

binarization means for comparing the digital signal with the threshold generated by the arithmetic means, and outputting a result of the comparison as the binary signal; and

latch means for latching the binary signal with the synchronous clock and outputting a synchronous signal, wherein

the arithmetic means ~~comprise~~ comprises:

threshold detection means for detecting a maximum value and a minimum value of the digital signal in a predetermined period, and outputting an average of the maximum value and the minimum value as the threshold;

rise time detection means for detecting a rise time as a time of intersection of the threshold and a line connecting two values of the digital signal, one of ~~which is~~ the two values being lower that the threshold and ~~the other~~ another of the two values being ~~which is~~ higher than the threshold, when the digital signal changes from the lower value to the higher value;

fall time detection means for detecting a fall time as a time of intersection of the threshold and a line connecting two values of the digital signal, one of the two values being ~~which is~~ higher than the threshold and ~~the other~~ another of ~~which is~~ the two values being lower than the threshold, when the digital signal changes from the higher value to the lower value;

input rate detection means for obtaining time intervals between ~~the~~ adjacent rise and ~~the~~ fall times during a predetermined period, and outputting a minimum value of the time intervals as an input rate of the input analog signal; and

synchronous clock output means for obtaining a half timing of the input rate after an edge of the input analog signal is detected on the basis of the input rate and the rise and fall times and outputting a first one of the synchronous clock at that timing, and obtaining a timing of the input rate after the first synchronous clock is output and outputting a second or later one of the synchronous clock at that timing.

Claim 3 **(Currently Amended)** [The digital PLL device of Claim 1] A clock generation apparatus comprising:

A/D conversion means for converting an input analog signal into a digital signal;

arithmetic means for generating a threshold used as a reference when binarizing the digital signal to generate a binary signal and a synchronous clock for sampling the binary signal, on the basis of the digital signal;

binarization means for comparing the digital signal with the threshold generated by the arithmetic means, and outputting a result of the comparison as the binary signal; and

latch means for latching the binary signal with the synchronous clock and outputting a synchronous signal, wherein

the arithmetic means ~~comprise~~ comprises:

threshold detection means for detecting integrals of the digital signal in a predetermined period, and outputting an average of the integrals as the threshold;

rise time detection means for detecting a rise time as a time of intersection of the threshold and a line connecting two values of the digital signal, one of ~~which is~~ the two values being lower than the threshold and ~~the other~~ another of ~~which is~~ the two values being higher than the threshold, when the digital signal changes from the lower value to the higher value;

fall time detection means for detecting a fall time as a time of intersection of the threshold and a line connecting two values of the digital signal, one of ~~which is~~ the two values being higher than the threshold and ~~the other~~ another of ~~which is~~ the two values

being lower than the threshold, when the digital signal changes from the higher value to the lower value;

input rate detection means for obtaining time intervals between ~~the~~ adjacent rise and ~~the~~ fall times during a predetermined period, and outputting a minimum value of the time intervals as an input rate of the input analog signal; and

synchronous clock output means for obtaining a half timing of the input rate after an edge of the input analog signal is detected on the basis of the input rate and the rise and fall times and outputting a first one of the synchronous clock at that timing, and obtaining a timing of the input rate after the first synchronous clock is output and outputting a second or later one of the synchronous clock at that timing.

Claim 4 **(Canceled)**

Claim 5 **(Currently Amended)** [The digital PLL device] The clock generation apparatus of Claim 2, further comprising:

an oversampling digital filter for interpolating ~~the~~ adjacent digital signals.

Claim 6 **(Currently Amended)** [The digital PLL device] The clock generation apparatus of Claim 3, further comprising:

an oversampling digital filter for interpolating ~~the~~ adjacent digital signals.